Application No.: 10/701,045
Reply to Office Action of May 13, 2005

REMARKS/ARGUMENTS

The above-identified patent application has been amended and re-examination and reconsideration are hereby requested.

Corrections to the specification have been made as required by the Examiner.

The claims have been amended to provide proper antecedent basis for the terms used therein.

Applicant respectfully requests reconsideration for the Examiner suggestion that the term "such" be changed to "said" or to "the". It is respectfully submitted that the claims are definite tuner 35 USC.

Before considering the claims and how they distinguish over the prior art cited by the Examiner, perhaps it might be helpful to review features of applicant's invention.

Referring to FIG. 1 an amplifier circuit 10 is provided having a transistor 12 for amplifying a radio frequency signal fed thereto, such amplified signal being coupled to a load, R_L. A processor 26 is provided to produce a control signal for the varactor which ***maximizes power fed to the transistor, as detected by the voltage produced across resistor R while minimizing power dissipated by such transistor, as detected by the output voltage across nodes N2 and N3 of bridge 16.*** With such arrangement, with the circuit 10 (FIG. 1), the use of an rf detector on the output of the transistor is avoided by providing a sensor for P_{dc} and P_{diss}. Here, the sensor for P_{dc} is the resistor R and the sensor for P_{diss} is the bridge 16. It is assumed that the DC voltage across the transistor is fixed.

Referring now to the cited art, and in particularly Burke et al., Burke et al., are trying provide proper feedback to achieve 180 degrees of phase shift and hence oscillation. Applicant, on the other hand ***maximizes power fed to the transistor, as detected by the voltage produced across resistor R while minimizing power dissipated by such transistor, as detected by the output voltage across nodes N2 and N3 of bridge 16.*** Nothing in Burke et al., suggests a system which uses a bridge to detect power dissipated by a transistor and combine it with a processor and loop to maximize power to a transistor while minimizing power dissipated by the transistor. Hence, nothing in either Kelly or Burke et al., taken either

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singly or in combination suggest such an arrangement; hence the Examiner has failed to establish a prima facie case of obviousness.

Referring now to the claims, the claims have been amended to point out that the claimed subject matter relates to an amplifier circuit having a transistor for amplifying a radio frequency signal fed thereto, such amplified signal being coupled to a load. The amplifier circuit includes a tuning circuit coupled between an output electrode of the transistor and the load. The tuning circuit has a tunable element controlled by a control signal fed to such tunable element. The amplifier also has an electrical device coupled between the voltage source and the transistor for providing a measure of power fed to the transistor. The amplifier also has a processor coupled to the electrical device and ***to output provided by the second node and the third node*** for producing the control signal.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-3192.

Respectfully submitted,

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Date

Richard M. Sharkansky
Attorney for Applicant(s)
Reg. No.: 25,800
P. O. Box 557
Telephone: (508) 477-4311
Facsimile: (508) 477-7234